REMARKS

The present application was filed on December 24, 2001 with claims 1-21. Claims 1, 7, 12, 16 and 19 are the independent claims. In the final Office Action, the Examiner: (i) maintained the rejection of claim 15 under 35 U.S.C. §112, second paragraph; (ii) maintained the rejection of claims 1, 5, 7, 10, 12, 15, 16 and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,330,684 to Yamanaka et al. (hereinafter "Yamanaka"); and (iii) maintained the rejection of claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 under 35 U.S.C. §103(a) as being unpatentable over Yamanaka.

In this response, Applicants respectfully reiterate their traversal of the various §112, §102(e), and §103(a) rejections for at least the reasons set forth in their Response to Office Action dated December 13, 2004.

Nonetheless, Applicants have amended independent claims 1, 7, 12, 16 and 19 in a sincere effort to expedite the present application through to issuance. More particularly, Applicants have amended claims 1, 7, 12, 16 and 19 by effectively incorporating therein the subject matter of dependent claims 3, 9, 14, 18 and 21, respectively. Claims 3, 9, 14, 18 and 21 have thus been canceled. Further, the dependency of claim 4 has been amended.

With regard to the issue of whether claim 15 is indefinite in accordance with §112, second paragraph, Applicants maintain that such is not the case with original claim 15. Nonetheless, Applicants have amended claim 15 to indicate that the Viterbi decoder comprises an integrated circuit device.

With regard to the issue of whether the claims of the present application are anticipated under 35 U.S.C. §102(e) by Yamanaka and/or unpatentable under 35 U.S.C. §103(a) over Yamanaka, Applicants assert that Yamanaka fails to teach or suggest all of the limitations in claims of the present application, and fails to provide proper motivation to be modified to achieve the claimed invention.

The present invention, for example, as recited in amended independent claim 1, recites a method of performing add-compare-select operations in accordance with a Viterbi decoder comprising the following steps. Input values of two or more sets of input values are respectively added to generate sums for the two or more sets. Substantially concurrent with the respective addition of the input values of the two or more sets of input values, the two or more sets of input values are compared. The comparison operation comprises performing carry save addition on the two sets of input values, and evaluating a carry output of the carry save addition operation to make

the determination as to which set of the two or more sets would yield a particular result (by way of example only, yields the largest sum). One of the generated sums of the two or more input sets is selected based on the comparison operation performed on the two or more sets of input values. Amended independent claims 7, 12, 16 and 19 recite similar limitations.

The Office Action at page 4 states that:

> Col. 13, lines 25-31 in Yamanaka teach that a carry operation is performed at comparator 26 of Figure 18 in Yamanaka (Note: carry is a standard operation in any ACS circuit), storing section 7 and 11 comprise and [sic] storage device for storing output of the comparators; hence combined with the comparators and adders comprise carry save addition circuitry for performing carry save addition.

While Applicants respectfully disagree with this rationale since Yamanaka neither teaches nor suggests use of any carry save addition in an ACS operation as performed in the claimed invention, Applicants further assert that the rejection fails to point out where Yamanaka teaches or suggests "evaluating a carry output of the carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result," as is also recited in accordance with the claimed invention.

As illustratively explained in the present specification at page 5, lines 14-22, and pointed out in Applicants' previous response, carry save operation is:

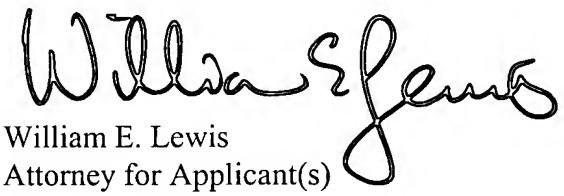
> [A]n approach used for the evaluation of multi-operand addition. A prime example is partial product summation in multipliers. In carry save addition, the time consuming carry propagations are not performed. Rather, the carries generated at various bit positions are saved as another binary number. For example, in a three operand addition involving a single level of full adders, two outputs from the full adder network, i.e., sum and carry, together represent the result. In order to form the final result as a single binary number, these binary numbers (sum and carry) should be added together (carry propagate addition). In contrast to carry propagate addition, carry save addition always produces results in sum and carry form, wherein each of the sum and carry are binary numbers themselves.

While column 13, lines 25-31, of Yamanaka mentions a carry input of comparator 26, no where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation that comprises evaluating a carry output of a carry save addition operation to make the determination as to which set of the two or more sets would yield a particular result, as recited in the claimed invention.

In fact, all Yamanaka states is that "[t]he comparing section 5 inputs two path metrics (PM1, PM0) from the bus 2 and two branch metrics (BM1, BM0) from the bus 4 so as to calculate PM1+BM1-PM0-BM0 . . . [and] the selecting section 8 inputs the most significant bit (hereinafter referred to as "MSB") which is the code bit of the comparison result of the comparing section 5, PM1+BM1-PM0-BM0" (see column 6, lines 25-36). This clearly implies that the comparison operation in Yamanaka performs a complete addition operation with carry propagate type addition such that the MSB is generated and available for use in the selection step (see carry propagate addition explanation repeated above from page 5, lines 14-22, of the present specification). This is significantly different than what the claimed invention recites.

In view of the above, Applicants believe that claims 1, 2, 4-8, 10-13, 15-17, 19 and 20 are in condition for allowance, and respectfully request withdrawal of the various §112, §102(e), and §103(a) rejections.

Respectfully submitted,



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